power from dissimilar diodes would require an optimization of equalizing networks for each individual diode.

VI. Conclusion

Based on the information presented in this paper, which is of a theoretical and experimental nature, it is now possible to design single as well as N-diode efficient and stable microwave oscillators. The oscillators designed using the techniques described within have delivered the highest, solid-state output power per diode at Ku-band frequencies to date.

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An 8–18-GHz YIG-Tuned FET Oscillator

JAMES C. PAPP, MEMBER, IEEE, AND YOSHIOMI Y. KOYANO

Abstract—**We report here on the design and construction of a YIG-tuned FET oscillator tunable over the entire 8–18-GHz frequency range. The minimum output power from this device operating into a 50-Ω load is about +6 dBm. The addition of a balanced buffer amplifier increases the power to about +12-dBm minimum. When optimized for the 12–18-GHz band, the oscillator alone generates a minimum of +10 dBm. The oscillator/amplifier combination produces at least +15 dBm. We discuss a number of difficulties inherent in the design of broad-band oscillators, especially fixed frequency resonances, linearity, and power drop outs at the low end of the frequency range.**

I. Introduction

BROAD-BAND TUNABLE oscillators operating at frequencies above 8 GHz have traditionally used bulk effect diodes as the active elements. With the introduction of 1-μm and 0.5-μm gate length field effect transistors (FET's) serious competition has developed for the diode oscillators. The improved efficiency and reliability of FET's compared to Gunn effect devices makes them especially attractive for application where low dc power consumption is important.

With only a few exceptions [1]–[4], [10] the literature on FET oscillators has concentrated on narrow band devices with bandwidths of less than 10 percent [5]–[9]. Only two papers [1], [10], presents design techniques of applicability to broad-band devices. Also, most work to date has been concentrated at frequencies below 12 GHz. Recently [13] work has been done in the 8–18-GHz range, however, the unbuffered oscillator module employed there produce substantially less power than the circuit described in this paper.

We present here the techniques employed in the design of a fundamental oscillator tunable by means of a YIG resonator over the entire 8–18-GHz frequency range. We also describe the construction details of the oscillator and finally present data on a typical unit.

II. Oscillator Design

Table I shows the common source S-parameters of the device initially chosen for this design, an NEC-388 FET manufactured by Nippon Electric Corporation. Since the measurements are done using a test fixture that closely resembles the final circuit, parasitic bonding inductances are already included in the S-parameters and need not be taken into account at a later stage in the design.

A typical oscillator topology is shown in Fig. 1. It consists of a YIG resonator described by a complex reflection coefficient Γ_R, a load characterized by a reflection coefficient Γ_L, and a circuit containing the active device which when connected to the load Γ_L is char-

Manuscript received December 10, 1979; revised February 7, 1980.
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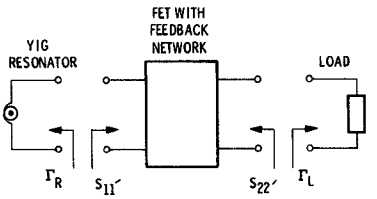


Fig. 1. Typical oscillator circuit topology with YIG resonator, active element, and matching network.

TABLE I
COMMON SOURCE S-PARAMETERS MEASUREMENT OF NEC-388 FET

FREQ (MHz)	S_{11} MAG	S_{11} ANG	S_{21} MAG	S_{21} ANG	S_{12} MAG	S_{12} ANG	S_{22} MAG	S_{22} ANG
8000.000	.760	-91	1.757	98	.075	41	.665	-39
9000.000	.758	-104	1.661	89	.073	40	.642	-49
10000.00	.755	-118	1.571	80	.071	39	.655	-57
11000.00	.756	-113	1.473	72	.067	35	.710	-64
12000.00	.701	-122	1.388	66	.060	50	.716	-64
13000.00	.677	-135	1.288	56	.061	45	.674	-71
14000.00	.670	-145	1.154	48	.063	51	.646	-81
15000.00	.685	-149	1.067	44	.057	57	.670	-88
16000.00	.723	-155	1.021	40	.112	59	.660	-95
17000.00	.709	-160	1.049	35	.105	29	.657	-94
18000.00	.720	-161	0.955	27	.086	22	.714	-96

Angular units are degrees

acterized by a reflection coefficient S_{11}'. The condition for oscillation to start is $\Gamma_R S_{11}' = 1$ or $\Gamma_L S_{22}' = 1$. The two conditions are equivalent [10] so we will employ only the first which is really two conditions:

$$|\Gamma_R||S_{11}'|e^{j(\theta_R + \theta_{S_{11}'})} = 1 \tag{1}$$

or

$$|\Gamma_R||S_{11}'| = 1 \tag{2}$$

and

$$\theta_R + \theta_{S_{11}'} = 0. \tag{3}$$

Equation (2) is the condition for steady-state oscillation. However, once oscillations begin, S_{11}' may change from the small signal values used here. Therefore, we take the condition for oscillation to start to be

$$|\Gamma_R||S_{11}'| > 1 \tag{4}$$

where S_{11}' is the small signal value. Oscillations will build from the small signal conditions until S_{11}' changes sufficiently to satisfy (2).

We will see in Section IV below that for a YIG resonator operating in the frequency band of interest $|\Gamma_R| \approx 1$. So we can take as the condition for oscillation

$$|S_{11}'| > 1. \tag{5}$$

III. The Feedback Scheme

The FET can be imbedded in a variety of circuits which produce sufficient feedback to satisfy (5). There are three possible series feedback circuits and three parallel feedback circuits shown in Fig. 2. The block labeled "X" is some reactive circuit.

Since the parallel feedback type circuits require dc blocks in the feedback area they are more susceptible than

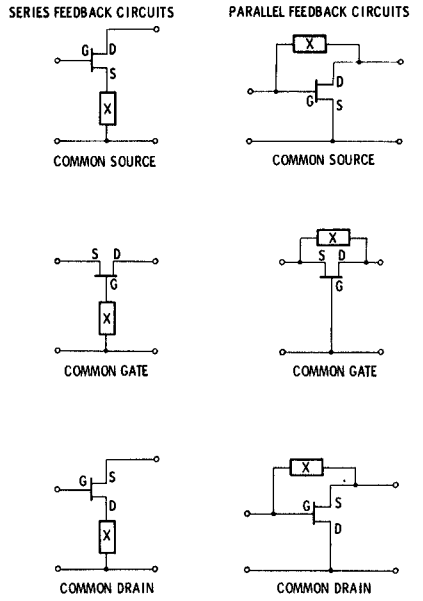
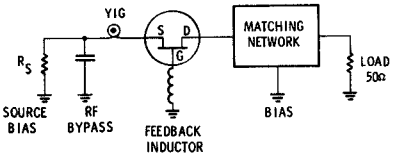
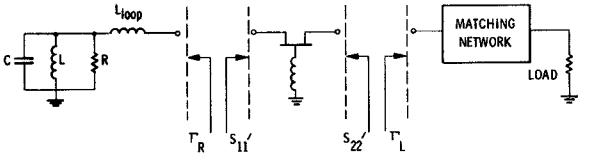


Fig. 2. Possible feedback schemes showing series and parallel type networks.



COMPLETE OSCILLATOR CIRCUIT



OSCILLATOR CIRCUIT WITH MODEL FOR RESONATOR. DC BIAS CIRCUIT HAS BEEN REMOVED SHOWING PARAMETERS OF INTEREST.

Fig. 3. Complete oscillator circuit including parallel resonant circuit model for YIG.

the series feedback circuits to problems due to parasitics which can be severe at 18 GHz. Inductive feedback is preferable to capacitive feedback because when constructed in microstrip the inductance of the feedback element is easy to adjust for optimum performance, while a capacitor value is difficult to change. Because the gate is run at 0 V dc we chose the common gate configuration over common source and common drain. This eliminates the need for any dc blocks or RF shorts in the feedback circuit thereby further eliminating parasitics. The complete circuit is shown in Fig. 3.

The first step in the design is the calculation of the common gate S-parameters of the FET for various values of feedback inductance [14]. Table II lists the S-parameters for 0.3, 0.5, and 1.0-nH inductance. Note that for 1 nH, $|S_{11}|$ is greater than 1 from about 9 GHz to 13 GHz so

TABLE II
COMMON GATE S-PARAMETERS

FREQ (MHz)	S_{11} MAG	S_{11} ANG	S_{12} MAG	S_{12} ANG	S_{21} MAG	S_{21} ANG	S_{22} MAG	S_{22} ANG
0.3 nH Feedback								
8000	0.319	177.7	0.149	49.39	1.313	-41.4	1.045	-25.7
10000	0.487	172.9	0.161	58.70	1.526	-61.5	1.269	-40.8
12000	0.586	159.2	0.194	79.80	1.798	-88.7	1.584	-55.4
14000	0.801	113.0	0.539	88.30	1.910	201.0	1.670	251.0
16000	0.754	88.7	0.755	74.35	1.630	150	1.430	212.0
18000	0.495	65.1	0.824	57.40	1.465	113	0.949	189.3
0.5 nH Feedback								
8000	0.438	170.0	0.124	66.8	1.450	-45.4	1.103	-27.1
10000	0.792	157.0	0.185	114.0	1.950	-74.0	1.490	-46.6
12000	1.219	124.3	0.536	121.6	2.830	239.0	2.100	-75.2
14000	0.919	53.8	0.943	62.7	1.850	140.0	1.151	209.0
16000	0.611	36.7	0.934	47.5	1.32	98.5	0.698	179.9
18000	0.433	181.0	0.191	48.6	1.21	77.7	0.383	169.0
1.0 nH Feedback								
8000	0.954	153.7	0.216	134.0	2.038	-59.4	1.335	-33.5
10000	2.690	84.47	1.378	103.2	4.154	210.0	2.300	257.1
12000	1.431	14.69	1.150	50.2	2.184	122.0	0.8114	200.0
14000	0.645	-0.248	0.897	34.7	1.099	78.2	0.172	191.0
16000	0.450	-5.43	0.883	29.6	0.976	56.2	0.0757	176.8
18000	0.386	-17.4	0.861	29.2	0.976	48.9	0.0528	-67.4

Angular units are degrees

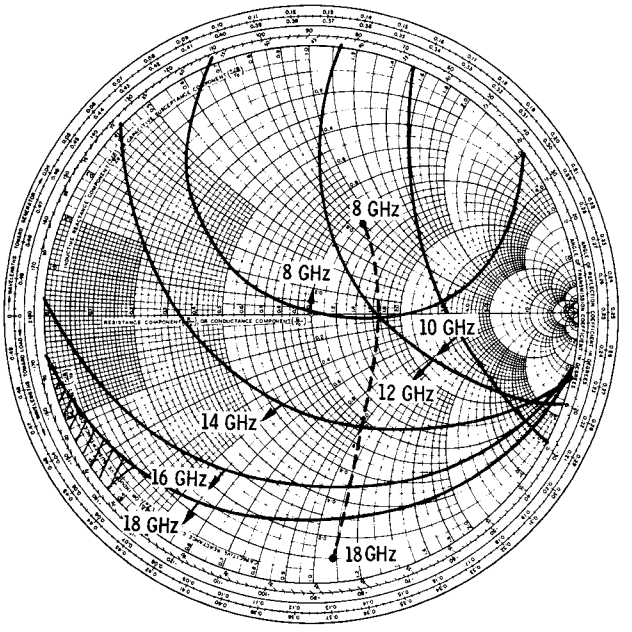


Fig. 4. Stability circles together with load trajector Γ_L across the 8–18-GHz range. Shaded area is the unstable region at 18 GHz referred to in the text.

oscillations will occur over this frequency range with no matching network at all—a 50-Ω load is all that is required in addition to the YIG resonator. As the inductance decreases, $|S_{11}|$ peaks at higher frequencies. However, there is no value of inductance that makes $|S_{11}|>1$ above 14 GHz. To obtain oscillation above 14 GHz a load other than 50 Ω must be placed at the drain.

If that drain load is characterized by a reflection coefficient Γ_L (see Fig. 3) then

$$S'_{11}=S_{11}+\frac{S_{12}S_{21}}{\frac{1}{\Gamma_L}-S_{22}}. \tag{6}$$

The objective then is to choose a Γ_L at all frequencies of interest so that $|S'_{11}|>1$ for a particular feedback inductance.

The values of Γ_L which satisfy this condition define a circle in the Γ_L plane [10]. This Γ_L circle can be constructed in two ways. First, (6) can be solved for Γ_L giving

$$\Gamma_L=\frac{S'_{11}-S_{11}}{S_{12}S_{21}+S'_{11}S_{22}-S_{11}S_{22}}. \tag{7}$$

Substituting in the known S-parameters and letting S'_{11} vary over all complex values of unit magnitude will produce the required circle. Alternatively one can solve for the location of the center of the circle, M, and its radius R by solving [11]

$$M=\frac{S^*_{22}-S_{11}(S^*_{11}S^*_{22}-S^*_{12}S^*_{21})}{|S_{22}|^2-|S_{11}S_{22}-S_{12}S_{21}|^2} \tag{8}$$

$$R=\frac{|S_{12}S_{21}|}{|S_{22}|^2-|S_{11}S_{22}-S_{12}S_{21}|^2}. \tag{9}$$

Once the circle is plotted the remaining task is to determine whether the region inside or outside the circle is the unstable ($|S'_{11}|>1$) one. This can be done immediately by noting that the center of the chart, $\Gamma_L=0$, corresponds to $S'_{11}=S_{11}$. Since S_{11} is known from Table II it is apparent whether the center of the chart is stable ($|S'_{11}|<1$) or unstable ($|S'_{11}|>1$). Since the circle divides the chart into two regions, the region which includes the center have the same stability as the center while the other region has the opposite stability. In Fig. 4 we have plotted these circles for 1-nH feedback inductance with arrows pointing toward the unstable region.

Also plotted in Fig. 4 is a trajectory of Γ_L with frequency that would be sufficient to produce oscillations across the 8–18-GHz range. The design problem then becomes the construction of a matching circuit that is described by a Γ_L similar to that in the figure.

A question relevant to the construction of the matching circuit is whether there are some loads that produce spurious oscillations. If the impedance presented to the YIG is sufficiently capacitive, a resonance with the inductive YIG coupling loop may occur producing a fixed frequency output. If the loop inductance is 1 nH the reflection coefficient of the resonator will be about $\Gamma_R=e^{j145°}$. So for a $\angle S_{11}\leqslant -145°$ there will be a possible spurious oscillation. At $|\Gamma_L|=1$ the condition $\angle S'_{11}\leqslant -145°$ corresponds to $\angle\Gamma_L\leqslant -139°$. So the shaded area in Fig. 4 is potentially unstable against spurious oscillation and should be avoided. Larger loop inductances make the spurious area larger.

IV. EFFECTS OF THE YIG

The YIG together with coupling loop is modeled in Fig. 3 as a parallel RLC circuit in series with an inductor. The elements values [12] are given by

$$L=\frac{R}{Q\omega_0} \tag{10}$$

$$C=\frac{1}{L\omega_0^2}=\frac{Q}{R\omega_0} \tag{11}$$

$$R=\mu_0\frac{V}{d^2}Q(2\pi\gamma)(4\pi M_s) \tag{12}$$

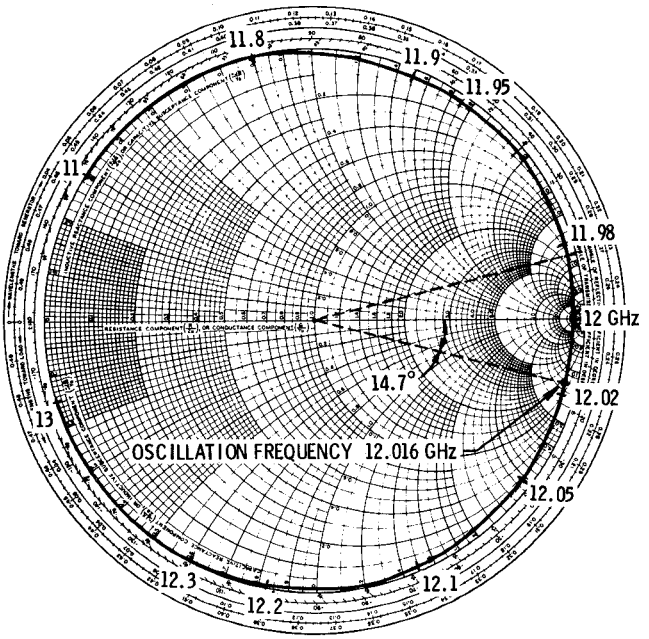


Fig. 5. Reflection coefficient Γ_R looking from the FET source toward the YIG near 12 GHz. Actual oscillation frequency is 12.016 GHz rather than 12.0 GHz.

where ω_0 is the frequency to which the YIG is tuned, V is the sphere volume, d is the diameter of the coupling loop, Q is the unloaded Q of the sphere, μ_0 is the permeability of free space, $4\pi \times 10^{-7}$ N/A^2, γ is the gyromagnetic ratio of the electron (2.8 MHz/gauss), and $4\pi M_s$ is the saturation magnetization of the resonator (1750 gauss in the case of pure YIG).

The impedance of the resonator becomes

$$Z_R(\omega) = \frac{R}{1+Q^2\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)^2} + j\left\{\omega L_{\text{Loop}} + \frac{RQ\left(\frac{\omega_0}{\omega}-\frac{\omega}{\omega_0}\right)}{1+Q^2\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)^2}\right\}. \quad (13)$$

Choosing a YIG diameter of 0.2 mm and a loop of 0.5 mm together with $Q=2000$ and 0.1-nH coupling loop inductance gives the result in Fig. 5 for Γ_R near 12 GHz. If the matching circuit at 12 GHz were chosen to be a 50-Ω load, $S'_{11}=S_{11}=1.43e^{j14.7°}$. Since the oscillation condition is $\angle\Gamma_R = -\angle S'_{11}$ the angle of Γ_R must be about $-14°$ giving an oscillation frequency of about 12.016 GHz instead of the 12 GHz to which the YIG is tuned. This phenomenon is called "pulling" and causes oscillator nonlinearity with tuning current. In order to improve the linearity it is necessary to spread the plot in Fig. 5 so that, for example, the 12.02-GHz point is moved to the location of the 12.05-GHz point. This brings the oscillation frequency at $-14°$ closer to ω_0. This spreading can be accomplished by decreasing R which in turn can be done by decreasing V/d^2 in (12). Physically this implies using a smaller sphere or larger loop. However, there is a limit to this procedure. As the frequency decreases to say 8 GHz, R decreases to 2/3 of its value at 12 GHz because R depends on Q which in turn depends linearly on frequency. As R gets smaller the locus in Fig. 5 gets closer to the center of the chart, decreasing $|\Gamma_R|$. Since we must have $|\Gamma_R||S_{11}|=1$ for oscillation, if $|\Gamma_R|$ decreases too much, the oscillation will cease. Thus the price of good linearity is the possibility of power dropouts at the low end of the frequency band.

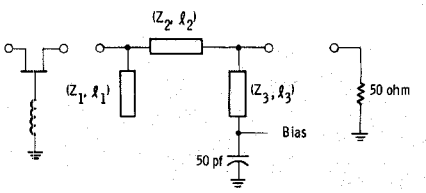


Fig. 6. Network chosen to provide 8–18-GHz match.

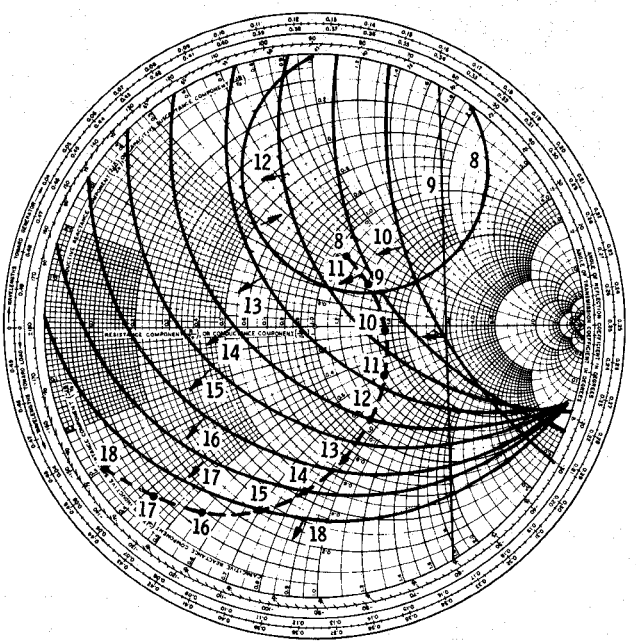


Fig. 7. Reflection coefficient Γ_L of matching network compared to stability circles from 8–18-GHz.

V. Design of the Circuit

Designing a circuit that produces a Γ_L like that in Fig. 4 is basically a trial and error procedure—no direct synthesis technique exists. The network chosen is shown in Fig. 6. The shorted stub provided the means for biasing the drain of the FET. The match provided by this circuit is shown in Fig. 7 plotted atop the stability circles that result from 0.6-nH feedback inductance.

VI. Circuit Construction

The circuit was fabricated using a 0.38-mm thick fused silica substrate using thin film MIC technology.

The unpackaged GaAs FET chip was die attached directly to a gold plated molybdenum carrier whose thermal coefficient of expansion approximates that of fused silica.

Molybdenum was used also because it is nonmagnetic.

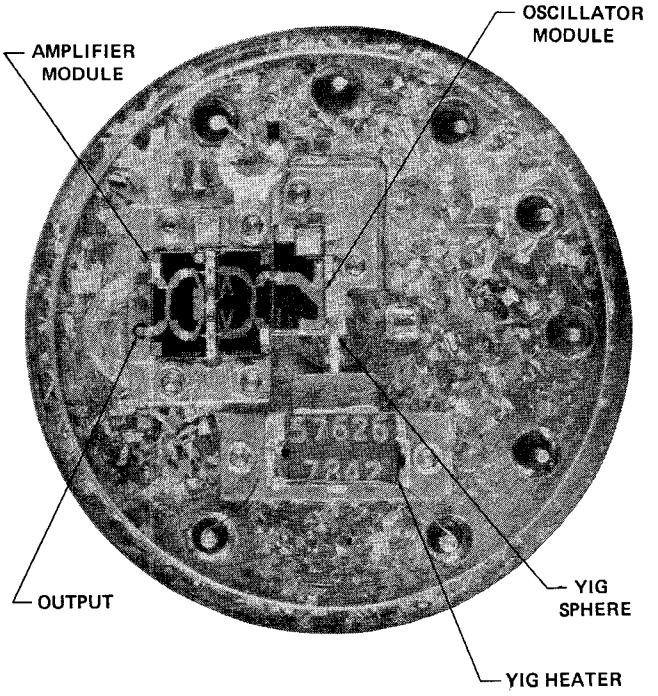


Fig. 8. Oscillator/buffer amplifier circuit constructed on fused silica.

To minimize the stray circuit parasitics, the FET was die attached as close as possible to the circuit with minimum lead lengths. Source inductance was minimized by using a 0.025-mm×0.635-mm gold ribbon for the YIG coupling loop and an Au wire mesh was used to bond from the source pad of the FET to the coupling loop. A 3-terminal chip voltage regulator was die attached to the circuit to provide a regulated bias voltage to the FET and also used to suppress any transients which could damage the FET.

An electronically regulated heater circuit was incorporated which provided temperature variations of less than ±1°C to the YIG sphere from −54°C to +85°C.

The entire circuit was enclosed in a magnetic shell housing which was hermetically sealed by welding.

Fig. 8 is a photograph of the oscillator circuit followed by a buffer amplifier which serves to improve the output power by about 5 dB and to provide 15 to 20 dB of isolation from load variations.

The transistor used in the construction had S-parameters similar to those used in the design stages with saturated drain-source current of $I_{DSS}=60$ mA and transconductance $g_m=40$ mmho.

VII. Results

Results of output power versus frequency are shown in Fig. 9. The power without the amplifier varies from +6-dBm minimum to +16-dBm maximum while the amplifier improves the output power by about 5 dB. Oscillations are obtained down to a frequency of 7.9 GHz and up to 18.5 GHz. Pushing the oscillation frequency as high as possible by varying the feedback inductance showed that the loop resonance was at 20.7 GHz. Tuning linearity was ±32 MHz.

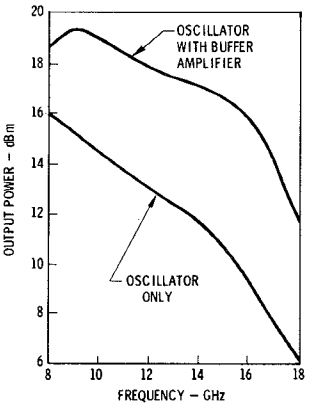


Fig. 9. Power output versus frequency across the 8–18-GHz band for the oscillator with and without buffer amplifier.

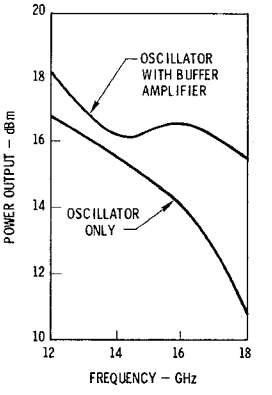


Fig. 10. Power output with the circuit optimized for the 12–18-GHz band.

With the gate inductance decreased and the circuit optimized for the 12–18-GHz band, minimum power improved to 10.8 dBm for the oscillator alone. Results are displayed in Fig. 10. The transistor operating conditions for all this data were about 50-mA I_{DS} and 5-V V_{DS} giving a peak efficiency of 16 percent.

VIII. Conclusions

Results have been presented on a YIG-tuned FET oscillator tunable over the entire 8–18-GHz frequency band producing a minimum of 11.8 dBm of power with a buffer amplifier. A general design technique was used which is applicable to wide-band transistor oscillators at all frequencies. Finally we have pointed out in detail the effects of the resonator circuit on linearity and low-frequency power dropouts and a means of avoiding spurious oscillations.

Acknowledgment

The authors wish to thank R. Suzuki for his work in aligning and tuning the oscillator and Dr. K. Niclas for help with a number of the calculations.

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The Design of Linearizing Networks for High-Power Varactor-Tuned Frequency Modulators

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Abstract—**The problem of linearizing the tuning varactor of a microwave frequency modulator is still a hard one to solve, and actual designs must often be carried out by trial-and-error techniques. A possible systematic approach to the solution of this problem, taking advantage of modern computer-aided design methods, is presented in this paper. It is shown that a suitable use of a general-purpose optimization program makes it possible to find a tuning network providing both FM linearity and protection of the varactor junction against an excess of RF voltage. This is of considerable importance in the case of medium- or high-power circuits, since the diode must then be prevented from being drawn into forward conduction or reverse breakdown for proper operation of the modulator.**

I. INTRODUCTION

THIS PAPER is concerned with the design of varactor-tuned frequency modulators (VTO's) of medium- or high-output power for use at microwave frequencies.

The problem of linearizing a varactor is a well-known one to microwave engineers, and considerable attention has been devoted to it in the literature. Several linearizing principles have been proposed, ranging from the introduction of a second resonator between the frequency-modulated oscillator and its load [1], [2] to the use of nonlinear feedback via harmonic tuning [3]. In most cases the way chosen to illustrate these concepts is to represent the tuned oscillator by a lumped negative-resistance equivalent circuit in order to make an analytical development possible. This usually cannot provide a complete and reliable picture of the nonlinear operation of the physical device, so that these methods have only limited practical application. Very often the actual design has to be carried out by empirical techniques, which is clearly unsatisfactory especially for MIC applications. The problem is further complicated when the oscillator to be modulated is medium- or high-power, since then an excess of RF voltage across the junction can break down the diode or draw it into forward conduction. If this is the case, empirically finding a solution may prove a lengthy and critical task.

A systematic approach to the design of varactor-tuned frequency modulators is attempted in this paper. Since the design of transistor oscillators, using both small- and large-signal S-parameters, has been widely discussed in the literature (e.g., [4]–[6]) and can be considered as a relatively settled matter, the emphasis here will be given to the modulation problem, i.e., changing a medium- or high-power fixed-frequency oscillator into a varactor-tuned FM source.

The basic idea is to embed the varactor diode in a lumped or distributed reactive network, which in principle allows the frequency-dependent tuning susceptance to be

Manuscript received January 15, 1979; revised January 16, 1980. Part of this work was presented at the 1978 IEEE MTT-S International Microwave Symposium, Ottawa, June 1978.

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0018-9480/80/0700-0767$00.75 ©1980 IEEE